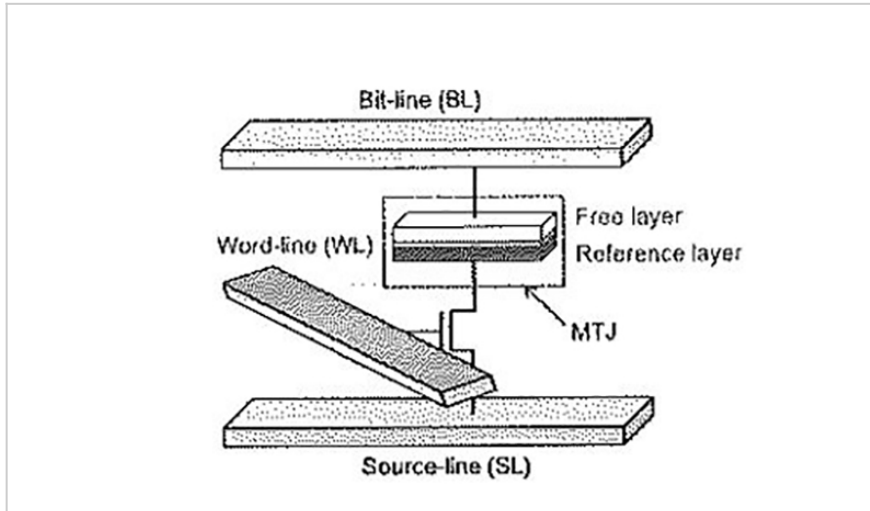


Improved STT-RAM L3 Caches Using Obstruction-Aware Cache Management

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View of STT-RAM Cell

Technology Summary

The disclosed invention describes an obstruction-aware cache management policy (OAP) to improve the performance and power efficiency of STT-RAM L3 caches. OAP adds monitors to the conventional cache architecture to periodically detect LLC-obstruction processes. LLC-obstruction processes are defined as workloads that cause significant degradation in the STT-RAM L3 based system. Based on the detection result, OAP controls L3 cache accesses from different processes to circumvent the obstructions.

Application & Market Utility

Enhances STT-RAM L3 cache performance; offsets the performance loss from asymmetric read/write. Technique allows for smaller area and lower energy consumption. STT-RAM L3 caches become an attractive option for future system design. A projected 4-core system (selected experimental subject) has its performance improved by an average of 14% and its energy consumption reduced by 64%. Covered by issued US Patent 9,223,716.

Next Steps

Seeking research collaboration and licensing opportunities.

TECHNOLOGY READINESS LEVEL

1-3

Seeking

Investment | Licensing | Research

Keywords

- STT-RAM
- LLC
- last level cache
- L3 cache
- spin-torque transfer

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